What is claimed is:

1. A process for growing a single crystal silicon ingot in which the ingot comprises a central axis, a seed-cone, a tail end, and a constant diameter portion between the seed-cone and the tail end having a lateral surface and a radius extending from the central axis to the lateral surface, the ingot being grown from a silicon melt and then cooled from the solidification temperature in accordance with the Czochralski method, the process comprising:

controlling a growth velocity, v, and an average axial temperature gradient, G_0, during the growth of the constant diameter portion of the crystal to form a segment which is axially symmetric about the central axis in which crystal lattice vacancies are the predominant intrinsic point defect, the segment having a radial width of at least about 25% of the radius; and,

cooling the ingot to form in the axially symmetric segment agglomerated vacancy defects and a residual concentration of crystal lattice vacancy intrinsic point defects, wherein the agglomerated vacancy defects have an average radius of less than about 70 nm and the concentration of residual crystal lattice vacancy intrinsic point defects is less than the threshold concentration at which uncontrolled oxygen precipitation occurs upon subjecting the cooled segment to an oxygen precipitation heat treatment.

2. The process of claim 1 wherein the ingot has a nominal diameter of at least 200 mm.

3. The process of claim 1 wherein the segment has a length, as measured along the central axis of the ingot, which is at least 20% of the length of the constant diameter portion of the ingot.

4. The process of claim 1 wherein the segment has a radial width of at least 75% of the radius of the constant diameter portion of the ingot.

5. The process of claim 4 wherein the ingot has a nominal diameter of at least 200 mm.

6. The process of claim 1 wherein the average void density is less than about 1×10^{8} cm^{-3}.

7. The process of claim 6 wherein the average void density is greater than about 5×10^{6} cm^{-3}.

8. The process of claim 1 wherein the average void density is greater than about 5×10^{6} cm^{-3}.

9. The process of claim 1 wherein the agglomerated vacancy defects have an average radius of less than about 50 nm

10. The process of claim 1 wherein the residual vacancy concentration is less than about 3×10^{12} cm^{-3}.

11. The process of claim 1 wherein the ingot has a nominal diameter of at least 200 mm, the segment has a length, as measured along the central axis of the ingot, which is at least 20% of the length of the constant diameter portion of the ingot, and a radial width of at least 50% of the radius of the constant diameter portion of the ingot.

12. The process of claim 11 wherein the average void density is less than about 1×10^{8} cm^{-3}.

13. The process of claim 12 wherein the average void density is greater than about 5 x 10^6 cm^{-3}.

14. The process of claim 11 wherein the average void density is greater than about 5 x 10^6 cm^{-3}.

15. The process of claim 11 wherein the agglomerated vacancy defects have an average radius of less than about 60 nm.

16. The process of claim 11 wherein the residual vacancy concentration is less than about 3 x 10^{12} $cm^{-3.}$

17. The process of claim 1 wherein the ingot is cooled at a first cooling rate through a first temperature range in which agglomerated vacancy defects are nucleated, and then at a second cooling rate through a second temperature range in which vacancy intrinsic point defects diffuse through the segment and are incorporated into nucleated agglomerated vacancy defects wherein the first cooling rate is greater than the second cooling rate.

18. The process of claim 17 wherein the first temperature range is from about 1000°C to about 1200°C.

19. The process of claim 17 wherein the second temperature range extends from about 900°C to about 1100°C.

20. A single crystal silicon wafer comprising a front surface, a back surface, a lateral surface joining the front and back surfaces, a central axis perpendicular to the front and back surfaces, and a segment which is axially symmetric about the central axis extending substantially from the front surface to the back surface in which crystal lattice vacancies are the predominant intrinsic point defect, the segment having a radial width of at

least about 25% of the radius and containing agglomerated vacancy defects and a residual concentration of crystal lattice vacancies wherein (i) the agglomerated vacancy defects have a radius of less than about 70 nm and (ii) the residual concentration of crystal lattice vacancy intrinsic point defects is less than the threshold concentration at which uncontrolled oxygen precipitation occurs upon subjecting the wafer to an oxygen precipitation heat treatment.

21. The wafer of claim 20 wherein the wafer is capable of having a concentration of oxygen precipitates of less than 1×10^{8} cm^{-3}, upon being subjected to a rapid thermal anneal in which the wafer is rapidly heated to a temperature of 1200°C in the essential absence of oxygen and then cooled, and then subjected to an oxygen precipitation heat treatment, consisting essentially of annealing said wafer at 800°C for 4 hours and then at 1000°C for 16 hours.

22. The wafer of claim 20 wherein said wafer has a nominal diameter of at least 200 mm.

23. The wafer of claim 20 wherein the segment has a width of at least 50% of the radius of the wafer.

24. The wafer of claim 20 wherein the segment has a width of at least 75% of the radius of the wafer.

25. The wafer of claim 20 wherein the segment has a width of at least 95% of the radius of the wafer.

26. The wafer of claim 20 wherein the agglomerated vacancy defects have an average radius of less than 60 nm.

27. The wafer of claim 20 wherein the agglomerated vacancy defects have an average radius of less than 50 nm.

28. The wafer of claim 20 wherein the agglomerated vacancy defects have an average radius of less than 40 nm.

29. The wafer of claim 20 wherein the agglomerated vacancy defects have an average radius of less than 30 nm.

30. The wafer of claim 20 wherein the average void density is less than 1×10^8 cm^{-3}.

31. The wafer of claim 20 wherein the average void density is less than 5×10^7 cm^{-3}.

32. The wafer of claim 20 wherein the average void density is less than 1×10^7 cm^{-3}.

33. The wafer of claim 20 wherein the average void density is less than 5×10^6 cm^{-3}.

34. The wafer of claim 20 wherein the average void density is greater than 5×10^6 cm^{-3}.

35. The wafer of claim 20 wherein the average void density is greater than 1×10^7 cm^{-3}.

36. The wafer of claim 20 wherein the average void density is greater than 5×10^7 cm^{-3}.

37. The wafer of claim 20 wherein the average void density is greater than 1×10^8 cm^{-3}.

38. The wafer of claim 20 wherein the oxygen content is less than 13 PPMA.

39. The wafer of claim 38 wherein the carbon concentration is less than 5×10^{16} atoms/cm^3.

40. The wafer of claim 39 wherein the nitrogen content is less than 1×10^{13} atoms/cm^3.

41. The wafer of claim 38 wherein the nitrogen content is less than 1×10^{13} atoms/cm^3.

42. The wafer of claim 20 wherein the carbon concentration is less than 5×10^{16} atoms/cm^3.

43. The wafer of claim 42 wherein the nitrogen content is less than 1×10^{13} atoms/cm^3.

44. The wafer of claim 20 wherein the nitrogen content is less than 1×10^{13} atoms/cm^3.

45. The wafer of any of claims 20-44 wherein the residual vacancy concentration is less than 3×10^{12} cm^{-3}.

46. The wafer of claim 20 wherein the residual vacancy concentration is less than 2×10^{12} cm^{-3}.

47. The wafer of claim 20 wherein the residual vacancy concentration is less than 1×10^{12} cm^{-3}.

48. The wafer of claim 20 wherein the residual vacancy concentration is less than 5×10^{11} cm^{-3}.

49. The wafer of claim 20 wherein the residual vacancy concentration is less than 1×10^{11} cm^{-3}.

50. The wafer of claim 20 wherein the residual vacancy concentration is less than 5×10^{10} cm^{-3}.

51. The wafer of claim 20 wherein the residual vacancy concentration is less than 1×10^{10} cm^{-3}.

52. The wafer of claim 20 wherein the wafer has a homoepitaxial layer deposited on the front surface thereof.

53. A method of evaluating gate oxide integrity of a population of single crystal silicon wafers, the method comprising (i) determining the dielectric breakdown characteristics of a first subset of said population as a function of the amount of stress applied to the first subset wherein the amount of stress is increased at a first rate from an initial value to a final value, (ii) determining the dielectric breakdown characteristics of a second subset of said population as a function of the amount of stress applied to the second subset wherein the amount of stress is increased at a second rate from an initial value to a final value and the second rate is different from the first rate, and (iii) using the dielectric breakdown characteristics determined in steps (i) and (ii) to predict the gate oxide failure rate under a defined set of conditions for the population.

54. The method of claim 53 wherein each of the subsets comprises a whole or fractional part of one or more wafers of the population.

55. The method of claim 53 wherein each of the subsets comprises a fractional part of the same wafers.

56. The method of claim 53 wherein each of the subsets comprises a fractional part of different wafers.

57. The method of claim 53 wherein a portion of each of the subsets comprises a fractional part of the same wafers.

58. The method of each of claims 53 to 57 wherein the dielectric breakdown characteristics are determined for four subsets of the populations of wafers.

59. The method of claim 53 wherein the rate of increase of each of said subsets differs from the rate of increase of the others by a factor of at least 10.